REMARKS/ARGUMENTS

Claims 1 through 50 are currently pending in the application.

Claims 1 through 16, 19 through 24, 26 through 41, and 44 through 50 stand rejected.

Claims 17, 18, 25, 42, and 43 have been withdrawn from consideration as being directed to non-elected inventions. Applicant has amended no claims, and respectfully requests reconsideration of the application herein.

Information Disclosure Statements

Applicant notes the filing of an Information Disclosure Statement herein on August 29, 2001, and of a Supplemental Information Disclosure Statement herein on August 22, 2002, and notes that no copies of the PTO-1449s were returned with the outstanding Office Action. Applicant respectfully requests that the information cited on the PTO-1449 be made of record herein.

Preliminary Amendment

Applicant's undersigned attorney notes the filing herein of a Preliminary Amendment on December 17, 2001, which filing was not acknowledged in the outstanding Office Action. Should the Preliminary Amendment have failed for some reason to have been entered in the Office file, Applicant's undersigned attorney will be happy to have a true copy thereof hand-delivered to the Examiner.

35 U.S.C. § 102(e) Rejections

Anticipation Rejection Based on U.S. Patent 6,410,415 to Estes

Claims 1, 3, 6, 8, 10, 12, 14, 16, 26, 28, 31, 33, 35, 37, 39 and 41 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Estes, U.S. Patent 6,410,415. Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant asserts that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The

identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Estes describes a semiconductor assembly comprising: a semiconductor device or a semiconductor die 1 having an active surface having at least one bond pad 6, a substrate 3 having an upper surface having at least one circuit, at least one bump 2 connecting one bond pad on said active surface of said semiconductor device 1 to said at least one circuit on said upper surface of said substrate 3, said at least one bump 2 forming a gap between said semiconductor device 1 and said substrate 3, and underfill material 5 provided between said substrate 3 and said semiconductor device 1.

In outstanding office action, it is asserted that Estes discloses at col. 17, lines 51-52 a wetting agent layer provided on the active surface of said semiconductor device (pg. 3). Applicant respectfully submits that Estes does not describe such. Rather, Estes describes that with chip heating maintained during the bonding, the adhesive wets the chip surface upon contact with the layer (col. 17, lines 51-52). Estes uses the term "wets" to mean to make wet, or to cover or coat with a liquid. Particularly, the adhesive will make wet, or cover or coat the chip surface upon contact with the layer. While it is true that a liquid may make wet a surface, it is not true that every liquid that wets a surface is a wetting agent. A wetting agent is a substance that when applied to a surface facilitates the prevention of that surface from repelling a wetting liquid. Practically, a wetting agent may be used to provide a greater capillary action of a liquid between surfaces to which the wetting agent has been applied. "Estes does not describe such a substance." Therefore, Applicant respectfully submits that Estes does not describe a wetting agent layer provided on the active surface of a semiconductor device, but rather an adhesive that covers or coats a chip surface and that is used to both secure the chip to the substrate and act as an underfill (col. 2, lines 14-24).

Independent claim 1 requires a semiconductor device comprising a semiconductor device having an active surface, at least a portion of said active surface having a wetting agent layer thereon.

As stated previously, Estes describes a semiconductor device 1 having an active surface and an adhesive 5 that makes wet the surface of the semiconductor device 1 (col. 17, line 52), but

does not identically describe, either expressly or inherently, the claim element of at least a portion of said active surface having a wetting agent layer thereon to anticipate the claimed invention under 35 U.S.C. § 102 of claim 1.

Because Estes does not identically describe, either expressly or inherently, each and every element as set forth in claim 1, Applicant respectfully requests that Examiner remove the rejection under 35 U.S.C. §102(e) directed at independent claim 1.

Applicant further submits that claim 3 is allowable as being dependent from an allowable base claim, in addition to any patentable subject matter contained therein.

Independent claim 6 claims a semiconductor assembly comprising a semiconductor device having an active surface, a substrate having an upper surface, and a wetting agent layer provided on one of said active surface of said semiconductor device and said upper surface of said substrate.

As stated previously, Estes describes a semiconductor device 1 having an active surface, a substrate 3 having an upper surface, and an adhesive 5 that wets a semiconductor device 1 (col. 17, line 52), but does not identically describe, either expressly or inherently, the claim element of a wetting agent layer provided on one of said active surface of said semiconductor device and said upper surface of said substrate to anticipate the claimed invention under 35 U.S.C. § 102.

Because Estes does not identically describe, either expressly or inherently, each and every element as set forth in claim 6, Applicant respectfully requests that the rejection under 35 U.S.C. §102(e) directed at independent claim 6 be withdrawn.

Applicant further submits that claim 8 is allowable as being dependent from an allowable base claim, in addition to any patentable subject matter contained therein.

Independent claim 10 states a semiconductor assembly comprising a semiconductor device having an active surface, a substrate having an upper surface, a wetting agent located on a portion of one of said active surface of said semiconductor device and said upper surface of said substrate, and an underfill material located between said substrate and said semiconductor device.

As previously stated, Estes describes a semiconductor device 1 having an active surface, a substrate 3 having an upper surface, an adhesive 5 that makes wet a semiconductor device 1 (col.

17, line 52), and an underfill material 5 located between said substrate 3 and said semiconductor device 1, but does not identically describe, either expressly or inherently, the claim element required by claim 10 of a wetting agent located on a portion of one of said active surface of said semiconductor device and said upper surface of said substrate to anticipate the claimed invention under 35 U.S.C. § 102.

Because Estes does not identically describe, either expressly or inherently, each and every element as set forth in claim 10, Applicant respectfully requests that the rejection under 35 U.S.C. §102(e) directed at independent claim 10 be withdrawn.

Applicant further submits that claim 12 is allowable as being dependent from an allowable base claim, in addition to any patentable subject matter contained therein.

Independent claim 14 requires a semiconductor assembly comprising a semiconductor device having an active surface having at least one bond pad thereon, another surface, a first end, a second end, a first lateral side and a second lateral side, a substrate having an upper surface having at least one circuit thereon, a first side wall, a second side wall, a first lateral side wall and a second lateral side wall, at least one bump connecting said at least one bond pad on said active surface of said semiconductor device to said at least one circuit on said upper surface of said substrate, said at least one bump forming a gap between said semiconductor device and said substrate, an underfill material provided between said substrate and said semiconductor device, and a wetting agent layer provided on at least a portion of one of said active surface of said semiconductor device and said upper surface of said substrate.

As previously mentioned, Estes describes a semiconductor device 1 having an active surface having at least one bond pad thereon, a substrate 3 having an upper surface having at least one circuit thereon (col. 1, line 14), at least one bump 2 connecting said at least one bond pad 6 on said active surface of said semiconductor device 1 to said at least one circuit on said upper surface of said substrate 3, said at least one bump 2 forming a gap between said semiconductor device 1 and said substrate 3, an underfill material 5 provided between said substrate 3 and said semiconductor device 1, and an adhesive 5 that makes wet the semiconductor device 1 (col. 17, line 52), but does not identically describe, either expressly or inherently, the claim element of a wetting agent layer provided on at least a portion of one of said

active surface of said semiconductor device and said upper surface of said substrate to anticipate the claimed invention under 35 U.S.C. § 102.

Because Estes does not identically describe, either expressly or inherently, each and every element as set forth in claim 14, Applicant respectfully requests that the rejection under 35 U.S.C. §102(e) directed at independent claim 14 be withdrawn.

Applicant further submits that claim 16 is allowable as being dependent from an allowable base claim, in addition to any patentable subject matter contained therein.

Independent claim 26 recites a semiconductor die comprising a semiconductor die having an active surface, at least a portion of said active surface having a wetting agent layer thereon.

Estes describes a semiconductor die 1 having an active surface and an adhesive 5 that makes wet a surface of the semiconductor die 1 (col. 17, line 52), but fails to disclose, either expressly or inherently, the claim element of at least a portion of said active surface having a wetting agent layer thereon.

Because Estes does not identically describe, either expressly or inherently, each and every element as set forth in claim 26, Applicant respectfully requests that the rejection under 35 U.S.C. §102(e) directed at independent claim 26 be withdrawn.

Applicant further submits that claim 28 is allowable as being dependent from an allowable base claim, in addition to any patentable subject matter contained therein.

Independent claim 31 claims a semiconductor assembly comprising a semiconductor die having an active surface, a substrate having an upper surface, and a wetting agent layer provided on one of said active surface of said semiconductor die and said upper surface of said substrate.

Estes describes a semiconductor die 1 having an active surface, a substrate 3 having an upper surface, and an adhesive 5 that makes wet a die 1 surface (col. 17, line 52), but fails to describe, either expressly or inherently, the claim element of a wetting agent layer provided on one of said active surface of said semiconductor die and said upper surface of said substrate.

Because Estes does not identically describe, either expressly or inherently, each and every element as set forth in claim 31, Applicant respectfully requests that the rejection under 35 U.S.C. §102(e) directed at independent claim 31 be withdrawn.

Applicant further submits that claim 33 is allowable as being dependent from an allowable base claim, in addition to any patentable subject matter contained therein.

Asserted in independent claim 35 is a semiconductor assembly comprising a semiconductor die having an active surface, a substrate having an upper surface, a wetting agent located on a portion of one of said active surface of said semiconductor die and said upper surface of said substrate, and an underfill material located between said substrate and said semiconductor die.

Described by Estes is a semiconductor die 1 having an active surface, a substrate 3 having an upper surface, an adhesive 5 that makes wet the die 1 surface (col. 17, line 52), and an underfill material 5 located between said substrate and said semiconductor. Nevertheless, Estes does not describe, either expressly or inherently, the element required by claim 35 of a wetting agent located on a portion of one of said active surface of said semiconductor die and said upper surface of said substrate.

Because Estes does not identically describe, either expressly or inherently, each and every element as set forth in claim 35, Applicant respectfully requests that the rejection under 35 U.S.C. §102(e) directed at independent claim 35 be withdrawn.

Applicant further submits that claim 37 is allowable as being dependent from an allowable base claim, in addition to any patentable subject matter contained therein.

Independent claim 39 recites a semiconductor assembly comprising a semiconductor die having an active surface having at least one bond pad thereon, another surface, a first end, a second end, a first lateral side and a second lateral side, a substrate having an upper surface having at least one circuit thereon, a first side wall, a second side wall, a first lateral side wall and a second lateral side wall, at least one bump connecting said at least one bond pad on said active surface of said semiconductor die to said at least one circuit on said upper surface of said substrate, said at least one bump forming a gap between said semiconductor die and said substrate, an underfill material provided between said substrate and said semiconductor die, and a wetting agent layer provided on at least a portion of one of said active surface of said semiconductor die and said upper surface of said substrate.

Estes describes a semiconductor assembly comprising a semiconductor die 1 having an active surface having at least one bond pad 6 thereon, a substrate 3 having an upper surface having at least one circuit thereon (col. 1, line 14), at least one bump 2 connecting said at least one bond pad 6 on said active surface of said semiconductor die 1 to said at least one circuit on said upper surface of said substrate 3, said at least one bump 2 forming a gap between said semiconductor die 1 and said substrate 3, an underfill material 5 provided between said substrate 3 and said semiconductor die 1, and an adhesive 5 that makes wet the die 1 surface, but does not describe, either expressly or inherently, the claim element of a wetting agent layer provided on at least a portion of one of said active surface of said semiconductor die and said upper surface of said substrate.

Because Estes does not identically describe, either expressly or inherently, each and every element as set forth in claim 39, Applicant respectfully requests that the rejection under 35 U.S.C. §102(e) directed at independent claim 39 be withdrawn.

Applicant further submits that claim 41 is allowable as being dependent from an allowable base claim, in addition to any patentable subject matter contained therein.

35 U.S.C. § 103(a) Rejections

Obviousness Rejection Based on U.S. Patent 6,410,415 to Estes in view of U.S. Patent 6,180,696 to Wong

Claims 2, 4 through 5, 7, 9, 11, 13, 15, 19, 27, 29 through 30, 32, 34, 36, 38, 40 and 44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Estes (U.S. Patent 6,410,415) in view of Wong (U.S. Patent 6,180,696). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.**

> The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Applicant respectfully submits that claims 2 and 4 through are in condition for allowance as depending from allowable base claim 1, in addition for the patentable subject matter contained therein.

Applicant respectfully submits that claims 7 and 9 are in condition for allowance as depending from allowable base claim 6, in addition for the patentable subject matter contained therein.

Applicant respectfully submits that claims 11 and 13 are in condition for allowance as depending from allowable base claim 10, in addition for the patentable subject matter contained therein.

Applicant respectfully submits that claims 15 and 19 are in condition for allowance as depending from allowable base claim 14, in addition for the patentable subject matter contained therein.

Applicant respectfully submits that claims 27 and 29 through 30 are in condition for allowance as depending from allowable base claim 26, in addition for the patentable subject matter contained therein.

Applicant respectfully submits that claims 32 and 34 are in condition for allowance as depending from allowable base claim 31, in addition for the patentable subject matter contained therein.

Applicant respectfully submits that claims 36 and 38 are in condition for allowance as depending from allowable base claim 35, in addition for the patentable subject matter contained therein.

Applicant respectfully submits that claims 40 and 44 are in condition for allowance as depending from allowable base claim 39, in addition for the patentable subject matter contained therein.

In addition, Estes fails to describe, teach or suggest the use of a wetting agent in conjunction with a semiconductor device or die to establish a *prima facie* case of obviousness

under 35 U.S.C. § 103 regarding the claimed invention. While Estes does teach or suggest an adhesive 5 wetting the surface of a semiconductor device 1 (col. 17, line 52), the adhesive 5 is not used as a wetting agent.

Wong teaches or suggests the use of ethyltrimethoxysilane as a coupling agent to improve the adhesion between the die and the underfill material and the underfill material and the substrate (col. 13, lines 37-40). Applicant respectfully submits that Wong does not teach or suggest ethyltrimethoxysilane as a wetting agent as asserted in the outstanding office action (pg. 3).

While the use of ethyltrimethoxysilane may facilitate good adhesion to chips and substrates, it is not used as a wetting agent as is required by the claimed invention. Wong teaches or suggests that a formulation including ethyltrimethoxysilane will have good wetting activity (col. 15, lines 18-22). Nevertheless, this wetting activity is much different than the effect that results from a wetting agent. Wetting activity, as is used in Wong and as generally known in the art, refers to the free flow of solder alloy on a metallic surface to produce an adherent bond, as is evinced by Wong's contextual teaching that a formulation containing ethyltrimethoxysilane shows good wetting activity to normal eutectic Sn/Pb solder bump (col. 17, lines 21-22). Hence, Wong does not teach or suggest the use of ethyltrimethoxysilane as a wetting agent; rather, Wong teaches ethyltrimethoxysilane as a coupling agent (col. 6, line 35).

There is no teaching or suggestion to make the claimed invention from either of the references of Estes and Wong or any combination thereof to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention because Wong does not use ethyltrimethoxysilane as a wetting agent, but rather as a coupling agent between surfaces, and Estes fails to describe, teach or suggest the use of a wetting agent in connection with a semiconductor device or die.

Therefore, it is respectfully submitted that Estes and Wong, individually and in any combination, at the very least, fail to teach or suggest all the claim limitations because neither teaches or suggests the use of a wetting agent, nor a specific wetting agent such as silane or ethyltrimethoxysilane to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention.

Further, the nonobviousness of independent claim 1 precludes a rejection of claims 2, 4, and 5 which depend therefrom, the nonobviousness of independent claim 6 precludes a rejection of claims 7 and 9 which depend therefrom, the nonobviousness of independent claim 10 precludes a rejection of claims 11 and 13 which depend therefrom, the nonobviousness of independent claim 14 precludes a rejection of claims 15 and 19 which depend therefrom, the nonobviousness of independent claim 26 precludes a rejection of claims 27, 29, and 30 which depend therefrom, the nonobviousness of independent claim 31 precludes a rejection of claims 32 and 34 which depend therefrom, the nonobviousness of independent claim 35 precludes a rejection of claims 36 and 38 which depend therefrom, and the nonobviousness of independent claim 39 precludes a rejection of claims 40 and 44 which depend therefrom because a dependent claim is obvious only if the independent claim from which it depends is obvious. *See* In re Fine, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988), *see also* MPEP § 2143.03. Therefore, the Applicant requests that the Examiner withdraw the 35 U.S.C. § 103(a) obviousness rejections from claims 2, 4 through 5, 7, 9, 11, 13, 15, 19, 27, 29 through 30, 32, 34, 36, 38, 40 and 44.

Obviousness Rejection Based on U.S. Patent 6,410,415 to Estes in view of U.S. Patent 6,190,940 to DeFelice

Claims 20, 21, 23, 24, 45, 46, 48 and 49 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Estes (U.S. Patent 6,410,415) in view of DeFelice (U.S. Patent 6,190,940). Applicant respectfully traverses this rejection, as hereinafter set forth.

DeFelice teaches or suggests a semiconductor assembly comprising a semiconductor die 21 and a substrate 37. DeFelice further teaches or suggests coating the substrate 37 with a layer of epoxy 39 to ensure wetting of the substrate 37 (col. 8, lines 4-5). DeFelice uses the term wetting to mean to cover with, or specifically, to cover with epoxy to facilitate the creation of a voidless underfill. As a practical matter, one who is bonding two surfaces together, such as a die and a substrate, would ensure the whole bonding surface is coated with epoxy to facilitate a more secure bond. This is in effect what DeFelice meant when it described coating the substrate with a layer of epoxy to ensure wetting of the substrate. DeFelice was concerned with achieving a stronger bond, not with preventing a surface from repelling a wetting liquid. Thus, DeFelice

does not teach or suggest a semiconductor device, die, or assembly comprising a wetting agent, a substance that when applied to a surface facilitates the prevention of that surface from repelling a wetting liquid.

Independent claim 20 requires a semiconductor assembly comprising a semiconductor device having an active surface, a substrate having an upper surface, an underfill material provided between said substrate and said semiconductor device, and a wetting agent layer provided on a portion of said active surface of said semiconductor device and a portion of said upper surface of said substrate.

Estes teaches a semiconductor device1 having an active surface, a substrate 3 having an upper surface, an underfill material 5 provided between said substrate 3 and said semiconductor device 1. Estes teaches an adhesive 5 wetting a semiconductor device 1 surface (col. 17, line 52) while DeFelice suggests wetting or coating the bonding surface of the substrate with epoxy (col. 8, lines 4-5). Nevertheless, Estes and DeFelice, individually and in any combination collectively, fail to teach or suggest a wetting agent layer provided on a portion of said active surface of said semiconductor device and a portion of said upper surface of said substrate to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention.

Therefore, it is respectfully submitted that, under 35 U.S.C. §103(a), independent claim 20 is allowable over the combination of Estes and DeFelice because the combination of the cited prior art, at the very least, does not teach or suggest the claim limitations of the claimed invention to establish a *prima facie* case of obviousness regarding the claimed invention under 35 U.S.C. §103(a).

Applicant respectfully submits that claim 21 is in condition for allowance as being dependent from an allowable base claim, in addition to the patentable subject matter contained therein.

Independent claim 23 teaches a semiconductor assembly comprising a semiconductor device having an active surface having a plurality of bond pads thereon, a substrate having an upper surface having a plurality of circuits thereon, a plurality of bumps connecting said plurality of bond pads on said active surface of said semiconductor device to said plurality of circuits on said upper surface of said substrate, said plurality of bumps forming a gap between said

semiconductor device and said substrate, an underfill material provided between said substrate and said semiconductor device, and a wetting agent layer provided on said active surface of said semiconductor device and on said upper surface of said substrate.

Estes teaches or suggests a semiconductor assembly comprising a semiconductor device 1 having an active surface having a plurality of bond pads 6 thereon, a substrate 3 having an upper surface having circuits thereon, a plurality of bumps 2 connecting said plurality of bond pads on said active surface of said semiconductor device 1 to said plurality of circuits on said upper surface of said substrate 3, said plurality of bumps 2 forming a gap between said semiconductor device 1 and said substrate 3, an underfill material 5 provided between said substrate 3 and said semiconductor device 1, but does not disclose a wetting agent layer provided on said active surface of said semiconductor device and on said upper surface of said substrate.

DeFelice teaches or suggests a semiconductor assembly comprising a semiconductor device 21, a substrate 37 with bonding sites 38, bonding sites 38 on the substrate 37 coated with a layer of epoxy 39 to ensure wetting of the substrate 37 with epoxy (col. 8, lines 4-5). Nevertheless, DeFelice does not teach a wetting agent layer provided on said active surface of said semiconductor device and on said upper surface of said substrate.

Therefore, it is respectfully submitted that, under 35 U.S.C. §103(a), independent claim 23 is allowable over the combination of Estes and DeFelice because the combination of the cited prior art, at the very least, does not teach or suggest the claim limitations of the claimed invention to establish a *prima facie* case of obviousness regarding the claimed invention under 35 U.S.C. §103(a).

Applicant respectfully submits that claim 24 is in condition for allowance as being dependant from an allowable base claim, in addition to the patentable subject matter contained therein.

Independent claim 45 claims a semiconductor assembly comprising a semiconductor die having an active surface, a substrate having an upper surface, an underfill material provided between said substrate and said semiconductor die, and a wetting agent layer provided on a portion of said active surface of said semiconductor die and a portion of said upper surface of said substrate.

Estes teaches or suggests a semiconductor die 1 having an active surface, a substrate 3 having an upper surface, an underfill material 5 provided between said substrate 3 and said semiconductor die 1, but does not teach or suggest a wetting agent layer provided on a portion of said active surface of said semiconductor die and a portion of said upper surface of said substrate.

DeFelice teaches or suggests a semiconductor assembly comprising a semiconductor die 21 having an active surface, a substrate 37 having an upper surface, bonding sites 38 on a substrate 37 being coated with a layer of epoxy 39 to ensure the wetting of the substrate 37 with epoxy (col. 17, lines 4-5), but fails to teach or suggest a wetting agent layer provided on a portion of said active surface of said semiconductor die and a portion of said upper surface of said substrate.

Therefore, it is respectfully submitted that, under 35 U.S.C. §103(a), independent claim 45 is allowable over any combination of Estes and DeFelice because the combination of the cited prior art, at the very least, does not teach or suggest the claim limitations of the claimed invention to establish a *prima facie* case of obviousness regarding the claimed invention under 35 U.S.C. §103(a).

Applicant respectfully submits that claim 46 is in condition for allowance as being dependant from an allowable base claim, in addition to the patentable subject matter contained therein.

Independent claim 48 teaches a semiconductor assembly comprising a semiconductor die having an active surface having a plurality of bond pads thereon, a substrate having an upper surface having a plurality of circuits thereon, a plurality of bumps connecting said plurality of bond pads on said active surface of said semiconductor die to said plurality of circuits on said upper surface of said substrate, said plurality of bumps forming a gap between said semiconductor die and said substrate, an underfill material provided between said substrate and said semiconductor die, and a wetting agent layer provided on said active surface of said semiconductor die and on said upper surface of said substrate.

Estes teaches or suggests a semiconductor assembly comprising a semiconductor die 1 having an active surface having a plurality of bond pads 6 thereon, a substrate 3 having an upper surface having a plurality of circuits thereon, a plurality of bumps 2 connecting said plurality of

bond pads 6 on said active surface of said semiconductor die 1 to said plurality of circuits on said upper surface of said substrate 3, said plurality of bumps 2 forming a gab between said semiconductor die 1 and substrate 3, an underfill material 5 provided between said substrate 3 and said semiconductor die 1. Nevertheless, Estes fails to teach or suggest a wetting agent layer provided on said active surface of said semiconductor die and on said upper surface of said substrate.

In addition, DeFelice fails to teach or suggest a wetting agent layer provided on an active surface of a semiconductor device and on an upper surface of a substrate.

Therefore, it is respectfully submitted that, under 35 U.S.C. §103(a), independent claim 48 is allowable over the combination of Estes and DeFelice because the combination of the cited prior art, at the very least, does not teach or suggest the claim limitations of the claimed invention to establish a *prima facie* case of obviousness regarding the claimed invention under 35 U.S.C. §103(a).

Applicant respectfully submits that claim 49 is in condition for allowance as being dependant from an allowable base claim, in addition to the patentable subject matter contained therein.

Obviousness Rejection Based on U.S. Patent 6,410,415 to Estes and U.S. Patent 6,190,940 to DeFelice and further in view of U.S. Patent 6,180,696 to Wong

Claims 22 and 47 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Estes (U.S. Patent 6,410,415) and DeFelice (U.S. Patent 6,190,940) as applied to claims 20 and 45 above, and further in view of Wong (U.S. Patent 6,180,696). Applicant respectfully traverses this rejection, as hereinafter set forth.

Dependent claim 22 requires the semiconductor assembly according to claim 20, wherein said wetting agent layer comprises one of silane, glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

As argued above, Applicant submits that independent claim 20 is in condition for allowance. Therefore, Applicant respectfully submits that claim 22 is allowable as being

dependent from allowable base claim 20, in addition to any patentable subject matter contained therein.

Dependent claim 47 claims the semiconductor assembly according to claim 45, wherein said wetting agent layer comprises one of silane, glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

As argued above, Applicant submits that independent claim 45 is in condition for allowance. Therefore, Applicant respectfully submits that claim 47 is allowable as being dependent from allowable base claim 45, in addition to any patentable subject matter contained therein.

Wong teaches or suggests the use of ethyltrimethoxysilane as a coupling agent which is used to improve the adhesion between the die and the underfill material and the underfill material and the substrate (col. 13, lines 37-40). Applicant respectfully submits that Wong does not teach ort suggest ethyltrimethoxysilane as a wetting agent as Examiner contends in the outstanding office action (pg. 5).

While the use of ethyltrimethoxysilane may facilitate good adhesion to chips and substrates, it is not used as a wetting agent as is required by Applicant's claims. Wong teaches or suggests a formulation including ethyltrimethoxysilane will have good wetting activity (col. 15, lines 18-22). Nevertheless, this wetting activity, as is used in Wong and as generally known in the art, refers to the free flow of solder alloy on a metallic surface to produce an adherent bond, as is evinced by Wong's contextual teaching that a formulation containing ethyltrimethoxysilane shows good wetting activity to normal eutectic Sn/Pb solder bump (col. 17, lines 21-22). Hence, Wong does not teach or suggest the use of ethyltrimethoxysilane as a wetting agent; rather, Wong teaches ethyltrimethoxysilane as a coupling agent (col. 6, line 35).

There is no teaching or suggestion to make the claimed invention from any combination of the references of Estes, DeFelice, and Wong. Wong does not teach or suggest using ethyltrimethoxysilane as a wetting agent, but rather as a coupling agent between surfaces. Additionally, Estes and DeFelice fail to describe, teach or suggest the use of a wetting agent in connection with a semiconductor device or die. Therefore, Estes, DeFelice, and Wong fail to teach or suggest all the claim limitations because neither teaches or suggests the use of a wetting

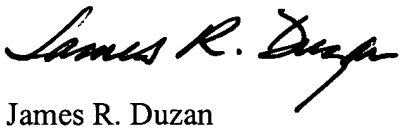
agent, nor a specific wetting agent such as silane or ethyltrimethoxysilane to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention.

Therefore, Applicant respectfully submits that Examiner remove the rejection, under 35 U.S.C. §103(a), from claims 22 and 47 because, at the very least, the prior art references do not teach or suggest all the claim limitations of the claimed invention to establish a *prima facie* case of obviousness under 35 U.S.C. §103(a), and because claims 22 and 47 depend from allowable base claims.

CONCLUSION

Claims 1 through 16, 19 through 24, 26 through 41, and 44 through 50 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,



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